REMARKS

Claims 2-5, 7-9, 13-16, 18-21, 23, 24, 26-28, and 33-42 are pending. Claims 2-5, 7-9, 13-16, 18-21, 23, 24, 26-28, and 33-41 are rejected. Claim 42 is newly added. No new matter is added.

Section 112, Second Paragraph Rejection

Claims 28, 35, and 38 are rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended claims 33 and 36 to expedite the prosecution of this patent application. Claims 28 and 35 depend from independent claim 33, and claim 38 depends from independent claim 36. Hence, for at least the reasons set forth above, Applicant respectfully requests that the Section 112 rejection of claims 28, 35, and 38 be withdrawn.

First 35 U.S.C. §103 Rejection

Claims 2, 5, 13, 18-21, 26-27, 33-34, 36-37, 39, and 41 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Chang et al. (U.S. Patent No. 6,269,467) ("Chang") in view of Bening et al. ("Optimizing Multiple EDA Tools within the ASIC Design Flow") ("Bening").

Independent clam 33 recites "interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types, wherein the selection of the particular type of interconnect is based on a probabilistic function", as claimed. In contrast, Chang teaches:

> glue logic must be optimally placed within the design to minimize wire congestion and timing complications which arise from placement of glue logic between blocks . . . First, glue logic that is not incorporated into predesigned blocks can be duplicated into multiple copies for distribution to the existing blocks. Second, logic that has no affinity to a block at the top level can be left as small blocks, optimally placed to minimize effective gate monopolization, wiring congestion, and floorplanning impact. Third, where the number of blocks exceeds the block place and

> route limitations, glue logic may be clustered into glue cluster blocks until the block count is reduced to an acceptable level.

(see col. 3, lines 4-7; col. 22, lines 2-11)

Applicant respectfully submits that Chang fails to teach or suggest that "the selection of the particular type of interconnect is based on a probabilistic function" because Chang discloses that the glue logic "must be optimally placed within the design to minimize wire congestion and timing complications". Moreover, Chang discloses that "glue logic that is not incorporated into predesigned blocks can be duplicated into multiple copies". Furthermore, Chang discloses that "logic that has no affinity to a block at the top level can be left as small blocks, optimally placed to minimize effective gate monopolization, wiring congestion, and floorplanning impact". Chang also discloses that "where the number of blocks exceeds the block place and route limitations, glue logic may be clustered into glue cluster blocks until the block count is reduced to an acceptable level". None of these ways of determining how to place glue logic teach or suggest a determination based "a probabilistic function", as claimed. For example, the determination to minimize "wire congestion and timing complications" is not an application of "a probabilistic function". Also, the determination that the glue logic "is not incorporated into predesigned blocks" is not an application of "a probabilistic function". Moreover, the determination that the "logic that has no affinity to a block at the top level" is not an application of "a probabilistic function". Also, the determination that "the number of blocks exceeds the block place and route limitations" is not an application of "a probabilistic function". Thus, Chang does not disclose or suggest the recitations of claim 33.

Moreover, Bening is not cited to teach or suggest "interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types, wherein the selection of the particular type of interconnect is based on a probabilistic function", as claimed. Rather, Bening is cited to teach "selecting a plurality of submodules from a design module library" (see Office Action, page 4). Hence, for at least the reasons set forth above, the combination of Chang and Bening does not teach or suggest the recitations of claim 33.

Moreover, for at least the same reasons set forth above, Applicant respectfully submits that claims 2, 5, 13, 18-21, 26-27, 34, 36-37, 39, and 41 are patentable over the combination of Chang and Bening.

Therefore, Applicant respectfully requests that the Section 103 rejection of Claims 2, 5, 13, 18-21, 26-27, 33-34, 36-37, 39, and 41 be withdrawn.

Second 35 U.S.C. §103 Rejection

Claims 4, 7-9, 15-16, and 23-24 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Chang in view of Bening and in further view of Zaidi (U.S. Patent Application Publication No. 2002/0038401 A1).

Claims 4, 7-9, 15, and 16 depend from independent claim 33. As explained above, the combination of Chang and Bening fails to teach or suggest a method as recited in claim 33. Moreover, Zaidi is not cited to disclose or suggest "interconnecting the lines of the plurality of parameterized submodules based on a selection of a particular type of interconnect from a plurality of interconnect types, wherein the selection of the particular type of interconnect is based on a probabilistic function", as claimed. Rather, Zaidi is cited to teach that "instantiation constraints are used to select the plurality of submodules" (see Office Action, page 5). Hence, for at least the reasons set forth above, claims 4, 7-9, 15, and 16 are patentable over the combination of Chang, Bening, and Zaidi.

For the reasons set forth above, Applicant respectfully submits that claims 23 and 24 are patentable over the combination of Chang, Bening, and Zaidi.

Therefore, Applicant respectfully requests that the Section 103 rejection of Claims 4, 7-9, 15-16, and 23-24 be withdrawn.

Third 35 U.S.C. §103 Rejection

Claims 28, 35, 38, and 40 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Chang in view of Bening in further view of Dustin ("Automated Testing Tools").

Claims 28 and 35 depend from independent claim 33. As explained above, the combination of Chang and Bening does not disclose or suggest a method as recited in claim 33. Moreover, Dustin is not cited to address the deficiencies of Chang and Bening with respect to independent claim 33. For example, Dustin is cited to teach "determining whether a predetermined number of test designs for testing the design automation tool has been generated . . . and applying the plurality of test designs to test the design automation tool" (see Office Action, page 7). Accordingly, Claims 28 and 35 are patentable over the cited combination at

least by virtue of their dependency.

For the same reasons set forth above, claims 38 and 40 are also patentable over the cited combination.

Therefore, Applicant respectfully requests that the Section 103 rejection of Claims 28, 35, 38, and 40 be withdrawn.

Fourth 35 U.S.C. §103 Rejection

Claim 14 is rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Chang in view of Bening in further view of Goossens ("Optimizing Multiple EDA Tools within the ASIC Design Flow").

Claim 14 depends from independent claim 33. As explained above, the combination of Chang and Bening fails to teach or suggest a method as recited in claim 33. Moreover, Goossens is not cited to address the deficiencies mentioned above with respect to Chang and Bening. For example, Goossens is cited to teach that "submodules comprise of adders and phase lock loops" (see Office Action, page 8). Accordingly, for at least these reasons, claim 33 and dependent claim 14 are patentable over the combination of Chang, Bening, and Goossens.

Fifth 35 U.S.C. §103 Rejection

Claim 3 is rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Chang in view of Bening and in further view of Rajsuman (U.S. Patent No. 6,678,645).

Claim 3 depends from independent claim 33. As described above, the combination of Chang and Bening fails to teach or suggest a method as recited in claim 33. Furthermore, Rajusman is not cited to cure the deficiencies in Chang and Bening. For example, Rajusman is cited to teach "generating a plurality of test designs of an ASIC including DSP and memory submodules" (see Office Action, page 9). Accordingly, for at least these reasons, Applicant respectfully requests that the Section 103 rejection of claim 3 be withdrawn.

New Claim

New claim 42, which depends from claim 33, is patentable over the cited art for at least the reasons set forth above.

Conclusion

In light of the above remarks, the rejections to the claims are believed overcome for at least the reasons noted above. Applicant believes that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
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